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(57) **ABSTRACT**

An electro-luminescence display panel and a driving method thereof for preventing a life shortening of the EL caused by a direct current are disclosed. In the electro-luminescence display panel implementing a gray level by a combination of light-emitting periods of sub-frames corresponding to each bit of video data, each of pixels includes an electro-luminescence (EL) cell, and a cell driver for allowing a forward current to be flown into the EL cell in accordance with a supplied data signal in a light-emitting period of the sub-frame while allowing a backward bias to be applied to the EL cell in a non-light-emitting period of the sub-frame.

(30) **Foreign Application Priority Data**

Mar. 31, 2004 (KR) P2004-022122

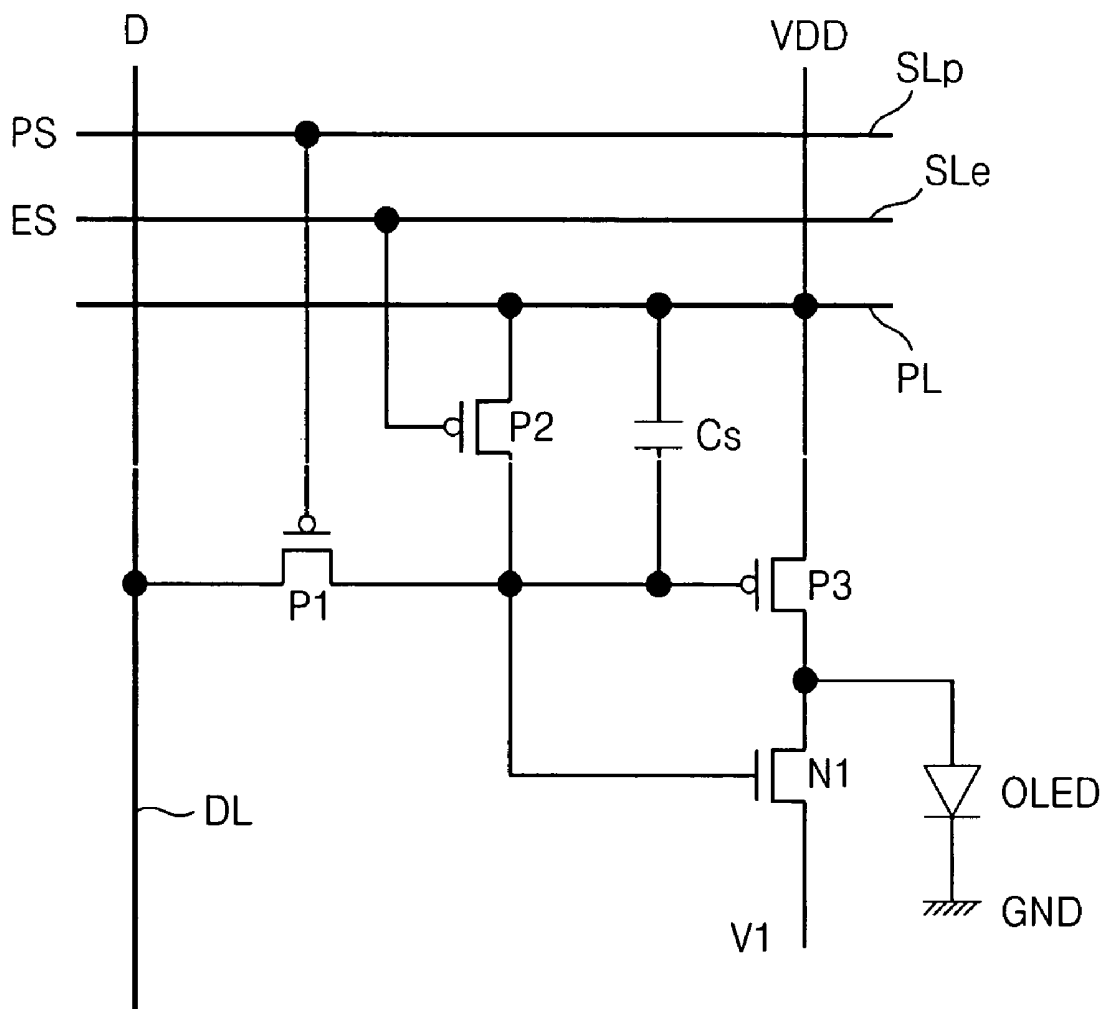


FIG. 1
RELATED ART

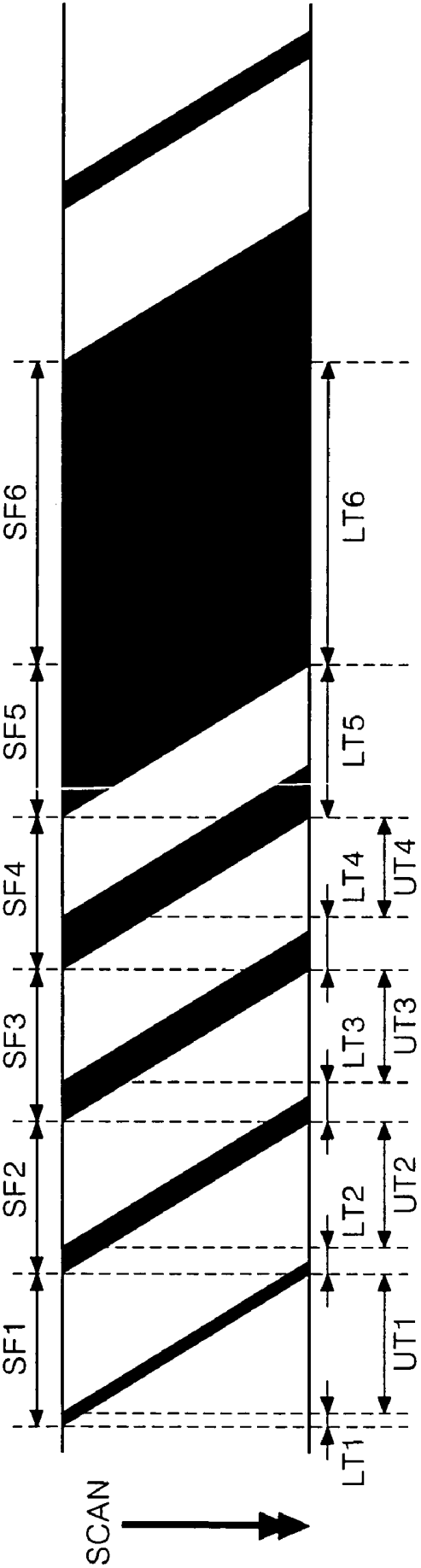
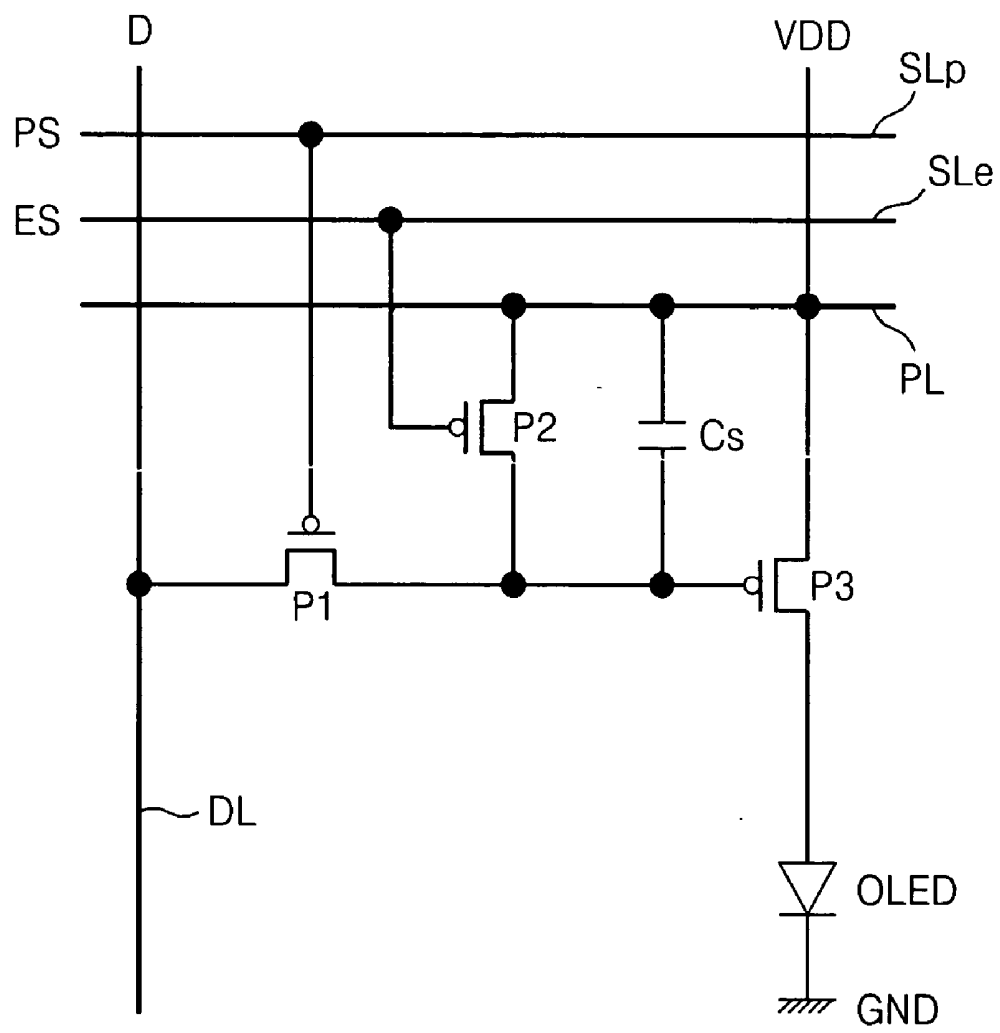


FIG.2
RELATED ART



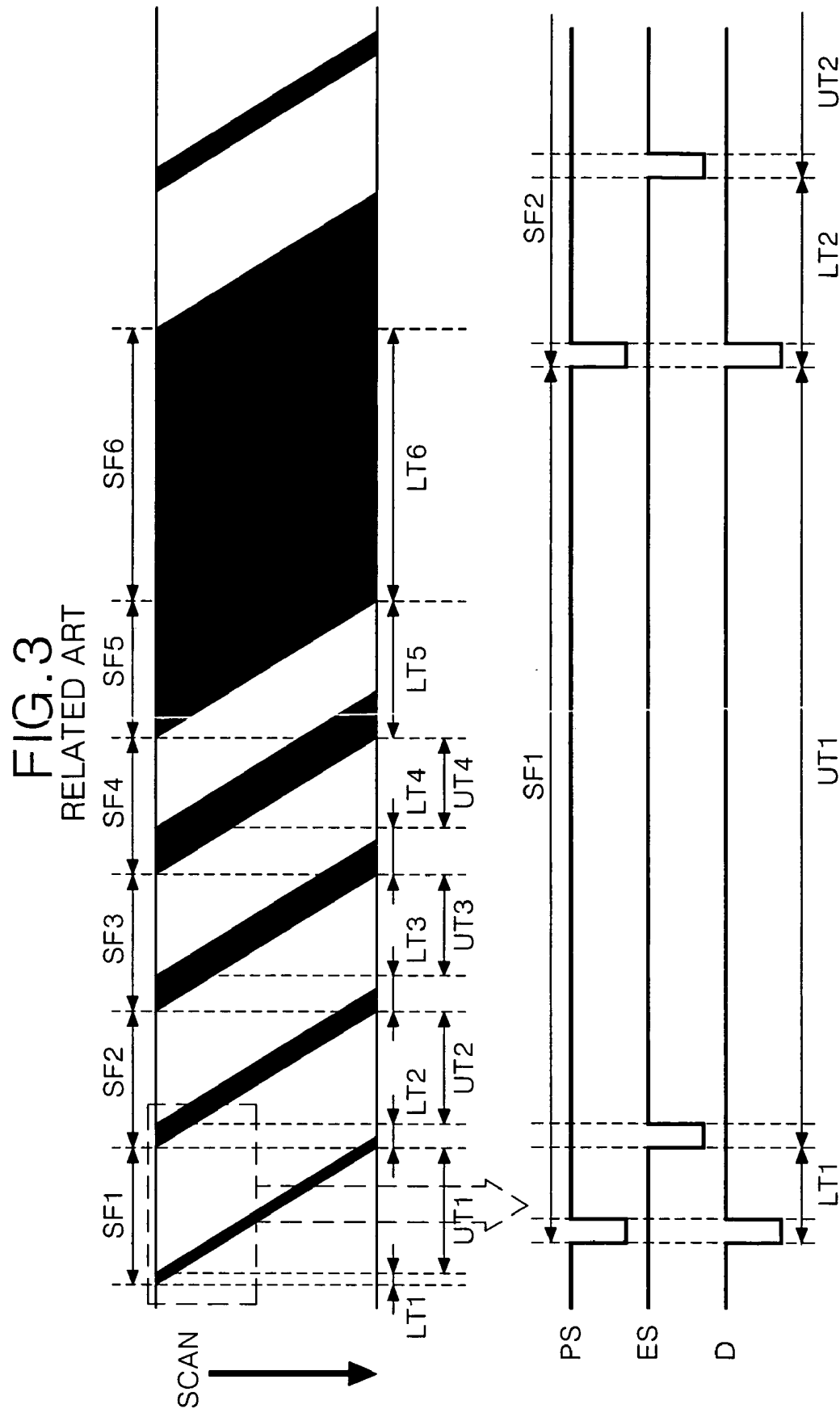


FIG. 4

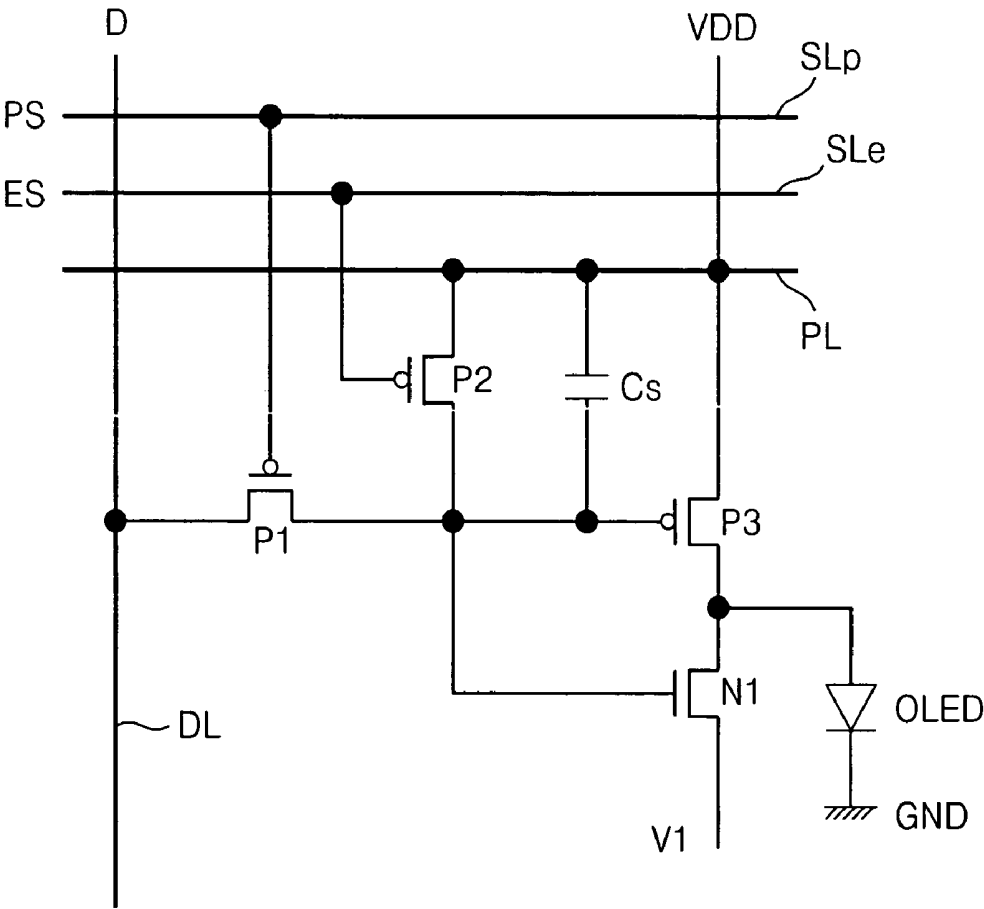


FIG. 5

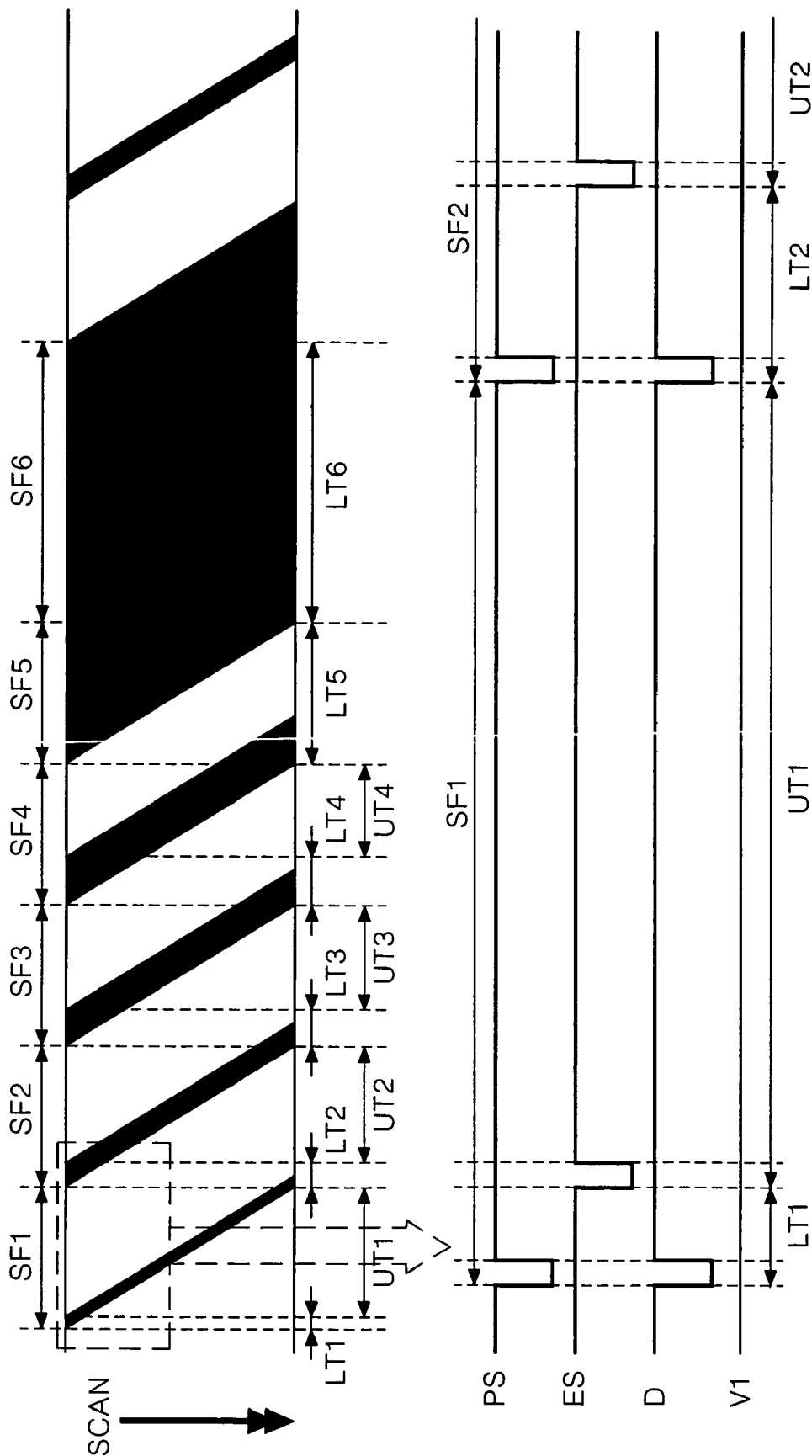


FIG.6

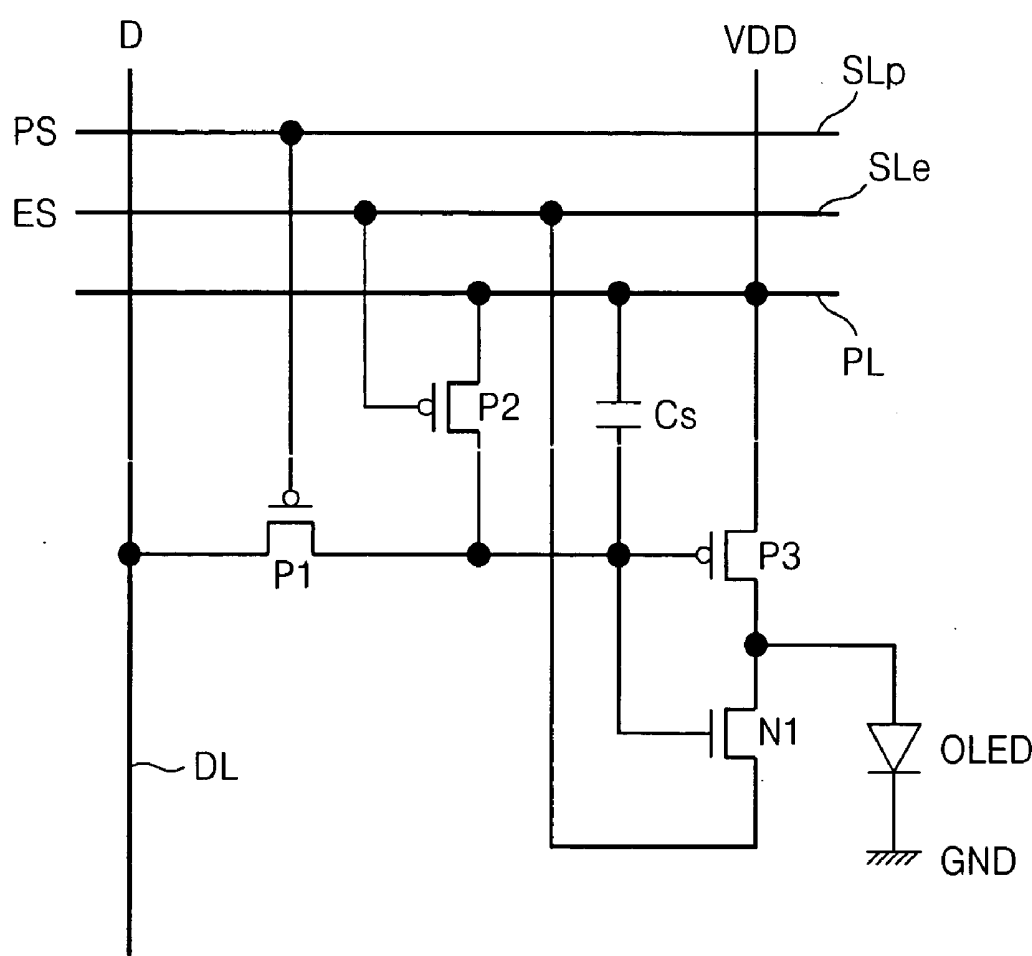
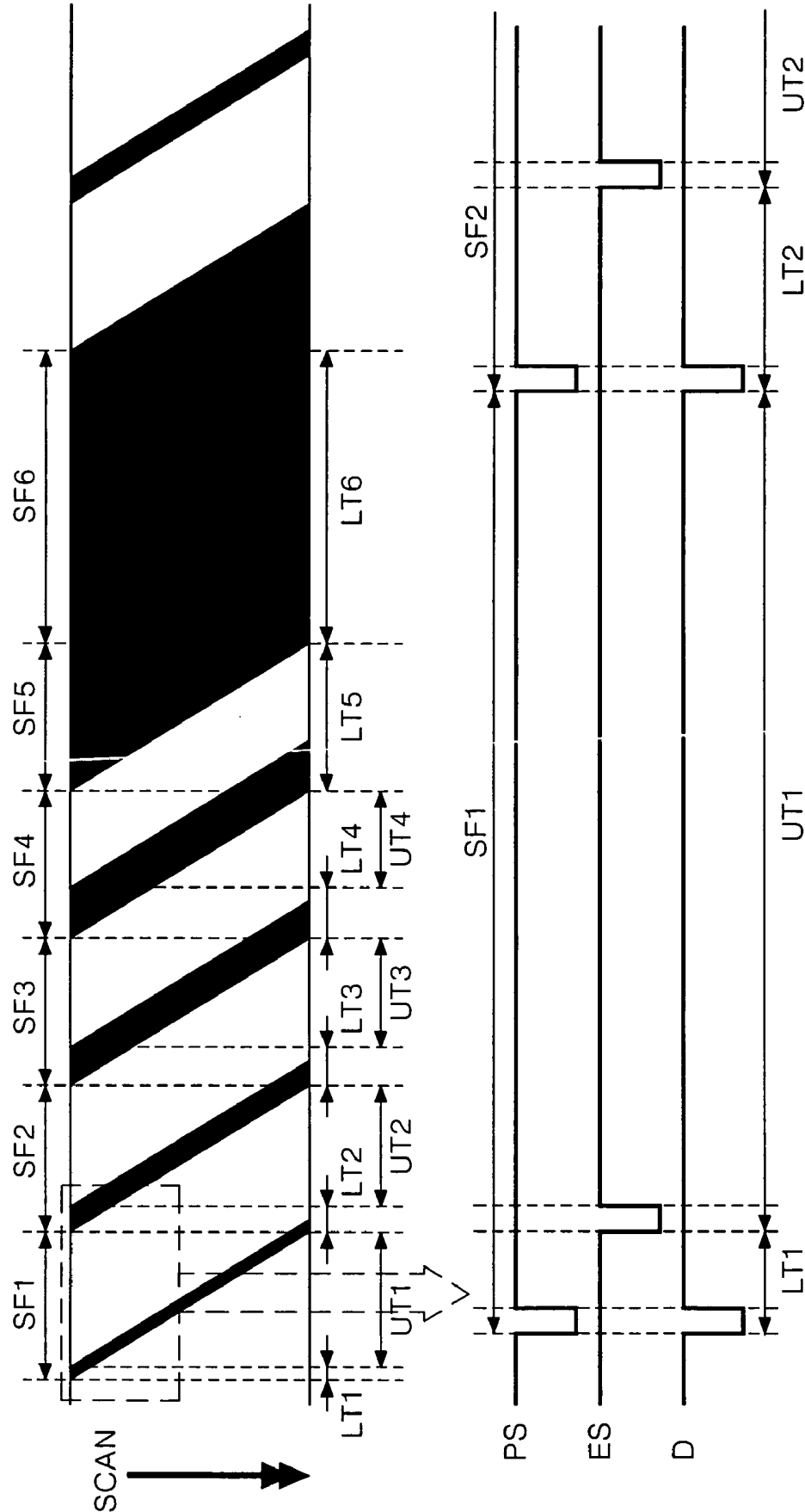


FIG. 7



ELECTRO-LUMINESCENCE DISPLAY PANEL AND DRIVING METHOD THEREOF

[0001] This application claims the benefit of Korean Patent Application No. P2004-22122 filed in Korea on Mar. 31, 2004, which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This invention relates to an electro-luminescence display (EL) display panel, and more particularly to an EL display panel and a driving method thereof that are adaptive for preventing a life shortening of the EL caused by a direct current (DC).

[0004] 2. Description of the Related Art

[0005] Recently, there have been highlighted various flat panel display devices reduced in weight and bulk that is capable of eliminating disadvantages of a cathode ray tube (CRT). Such flat panel display devices include a liquid crystal display (LCD), a field emission display (FED), a plasma display panel (PDP) and an electro-luminescence (EL) display panel, etc.

[0006] The EL display panel of such display devices is a self-luminous device capable of light-emitting a phosphorous material by a re-combination of electrons with holes. The EL display device is generally classified into an inorganic EL device using an inorganic compound as the phosphorous material and an organic EL device using an organic compound as it. Such an EL display panel can be driven a low driving voltage (e.g., 10V) unlike other display devices, and has an excellent recognition because it employs a self-luminescence. Also, the EL display panel can implement an ultra thin film device because it does not need a back light unlike the LCD. Furthermore, the EL display panel has advantages of a wider viewing angle and a faster response speed in comparison to the LCD such that it can be highlighted into a post-generation display device.

[0007] The organic EL device is usually comprised of an electron injection layer, an electron carrier layer, a light-emitting layer, a hole carrier layer and a hole injection layer that are disposed between a cathode and an anode. In such an organic EL device, when a predetermined voltage is applied between the anode and the cathode, electrons produced from the cathode are moved, via the electron injection layer and the electron carrier layer, into the light-emitting layer while holes produced from the anode are moved, via the hole injection layer and the hole carrier layer, into the light-emitting layer. Thus, the electrons and the holes fed from the electron carrier layer and the hole carrier layer emit a light by their re-combination at the light-emitting layer.

[0008] An active matrix EL display panel employing such an organic EL device is largely classified into an analog driving method and a digital driving method.

[0009] The analog driving method of the EL display panel is a driving method that controls a current amount fed to an EL cell by an analog signal having a different level in accordance with a video data signal, that is, by a voltage or current, thereby controlling brightness. [0008] On the other hand, the digital driving method of the EL display panel is a driving method that controls a light-emitting time of the EL cell according to a digital video data signal, thereby

controlling brightness. In this case, in order to control a light emitting period of the EL cell, one frame is divided into 1st to 6th sub-frames SF1 to SF6 when it is intended to a plurality of sub-frames corresponding to each bit of video data, that is, 6-bit video data as shown in FIG. 1. Further, since different weighting values are given to light-emitting periods of the 1st to 6th sub-frames SF1 to SF6, a ratio LT1:LT2:LT3:LT4:LT5:LT6 of the light-emitting periods of the 1st to 6th sub-frames SF1 to SF6 becomes 1:2:4:8:16:32. The 1st to 4th sub-frames SF1 to SF4 other than the 5th and 6th sub-frames SF5 and SF6 includes non-light-emitting periods UT1, UT2, UT3 and UT4 that are gradually decreased in opposition to the light-emitting periods LT1, LT2, LT3 and LT4. The EL cells arranged in a matrix type at the EL display panel are scanned, on a line sequence basis, in each light-emitting period LT1 to LT6 of the 1st to 6th sub-frames SF1 to SF6 to be turned on in accordance with a data signal, thereby providing a light-emission. On the other hand, the EL cells are scanned, on a line sequence basis, in each non-light-emitting period UT1 to UT4 of the 1st to 4th sub-frames SF1 to SF4 to be turned off, thereby stopping a light-emission. Accordingly, brightness of the EL device is implemented by combining light-emitting times of the sub-frames turned on in accordance with video data.

[0010] FIG. 2 is a detailed circuit diagram of one pixel configuring an active matrix EL display panel for providing a digital driving. FIG. 3 is a driving timing diagram of the first sub-frame SF1.

[0011] The pixel shown in FIG. 2 is comprised of an EL cell OLED, and a cell driver including three PMOS transistors P1, P2 and P3 and a storage capacitor Cs for driving the EL cell OLED.

[0012] The cell driver includes a storage capacitor Cs connected to a power line PL, a first switching PMOS transistor P1 connected between a data line DL and the storage capacitor Cs to be controlled by a light-emitting scan line SLp, a second switching PMOS transistor P2 connected between the power line PL and the storage capacitor Cs to be controlled by a non-light-emitting scan line SLe, and a third driving PMOS transistor P3 connected between a voltage supply line VDD and the EL cell OLED to be controlled by the storage capacitor Cs.

[0013] A writing scan line SLp provides a writing signal, that is, a program signal PS for turning on the first PMOS transistor P1 in a light-emitting period LT of each sub-frame SF. The first PMOS transistor P1 is turned on by the program signal PS to charge a data signal into the storage capacitor Cs, thereby turning on or off the third PMOS transistor P3 in accordance with the charged voltage during the light-emitting period LT.

[0014] An erasing scan line SLe provides an erasing signal ES for turning on the second PMOS transistor P2 in a non-light-emitting period UT of each sub-frame SF. The second PMOS transistor P2 is turned on by the erasing signal SE to discharge the storage capacitor Cs, thereby turning on the third PMOS transistor P3 during the non-light-emitting period UT.

[0015] Referring to FIG. 3, the first PMOS transistor P1 is turned on by a low voltage of the program signal PS in the non-light-emitting period LT1 of the 1st sub-frame SF1. Further, a low voltage ("0") or a high voltage ("1") of the

data signal is supplied via the turned-on first PMOS transistor P1 to be charged in the storage capacitor Cs. When the low voltage is charged in the storage capacitor Cs, the third PMOS transistor P3 is turned on to thereby turn on, that is, light-emit the EL cell OLED during the light-emitting period LT. On the other hand, when the high voltage is charged in the storage capacitor Cs, the third PMOS transistor P3 does not turn off, that is, light-emit the EL cell OLED during the light-emitting period LT.

[0016] Then, the second PMOS transistor P2 is turned on by a low voltage of the erasing signal SE in the non-light-emitting period UT1 to supply a high-level voltage VDD from the power line PL to a gate electrode of the third PMOS transistor P3, thereby discharging the storage capacitor Cs. Thus, the third PMOS transistor P3 is turned off, thereby allowing the EL cell OLED to be turned off, that is, to provide a non-light-emission in the non-light-emitting period UT.

[0017] However, the related art EL display panel has a problem in that, since it allows a current to be flown only in a forward direction (i.e., anode→cathode) at the EL cell for the purpose of light-emitting the EL cell OLED, a life of the EL cell OLED is shortened due to a direct current (DC).

[0018] Furthermore, the EL display panel driven by the digital driving method as shown in FIG. 2 also has a problem in that, since it allows a forward direction current to be flown into the EL cell OLED in accordance with a data signal in the light-emitting period LT while allowing a current to be not flown into the EL cell OLED by floating the anode of the EL cell OLED in the non-light-emitting period UT, a life of the EL cell OLED is shortened due to a direct current (DC).

SUMMARY OF THE INVENTION

[0019] Accordingly, it is an object of the present invention to provide an EL display panel and a driving method thereof wherein a backward bias can be applied to an EL cell in a non-light-emitting period of each sub-frame, thereby preventing a life shortening of the EL device caused by a direct current.

[0020] In order to achieve these and other objects of the invention, an electro-luminescence display panel according to one aspect of the present invention implements a gray level by a combination of light-emitting periods of sub-frames corresponding to each bit of video data, wherein each of pixels includes an electro-luminescence (EL) cell; and a cell driver for allowing a forward current to be flown into the EL cell in accordance with a supplied data signal in a light-emitting period of the sub-frame while allowing a backward bias to be applied to the EL cell in a non-light-emitting period of the sub-frame.

[0021] In the electro-luminescence display panel, the cell driver includes a storage capacitor having one electrode connected to a power line; a first switching transistor connected between a data line for supplying said data signal and other electrode of the storage capacitor to be controlled by a writing scan line for supplying a writing signal; a second switching transistor connected to the power line and other electrode of the storage capacitor to be controlled by an erasing scan line for supplying an erasing signal; a driving transistor connected between the power line and the EL cell

to be controlled by the storage capacitor; and a backward bias transistor connected between the driving transistor and a backward bias voltage input line to be controlled by the storage capacitor in opposition to the driving transistor.

[0022] Herein, the first switching transistor is turned on by said writing signal in the light-emitting period to charge said data signal into the capacitor, and the second switching transistor is turned on by said erasing signal in the non-light-emitting period to discharge said data signal charged in the capacitor.

[0023] The driving transistor turned on or off in accordance with said voltage charged in the capacitor in the light-emitting period while being turned off by said discharge of the capacitor in the non-light-emitting period, and allows said forward current to be flown into the EL cell when it is turned on in the light-emitting period.

[0024] The backward bias transistor is turned on in opposition to the driving transistor in the non-light-emitting period, thereby applying said backward bias to the EL cell.

[0025] Further, the backward bias transistor is turned on when the driving transistor is turned off by said data signal charged in the capacitor in the light-emitting period, thereby applying said backward bias to the EL cell.

[0026] The backward bias input line is identical to the erasing scan line.

[0027] The erasing scan line applies a turn-on voltage of the second switching transistor as said erasing signal in the non-light-emitting period, and said backward bias is applied, via the backward bias transistor, to the EL cell during a period when said turn-on voltage of said erasing signal is applied.

[0028] The first and second switching transistors and the driving transistor are PMOS transistors, and the backward bias transistor is a NMOS transistor.

[0029] A method of driving an electro-luminescence display panel according to another aspect of the present invention implementing a gray level by a combination of light-emitting periods of sub-frames corresponding to each bit of video data includes the steps of allowing a forward current to be flown into an electro-luminescence (EL) cell in accordance with a data signal in a light-emitting period of the sub-frame; and allowing a backward bias to be applied to the EL cell in a non-light-emitting period of the sub-frame.

[0030] In the method, said light-emitting period includes allowing said backward bias to be applied to the EL cell when a non-light-emitting data signal for non-light-emitting the EL cell by said data signal is supplied.

[0031] Herein, said light-emitting period includes allowing said data signal to be charged, via the first switching transistor, to a capacitor by a writing scan signal from a writing scan line; and turning on a driving transistor in accordance with a voltage charged in the capacitor, thereby allowing said forward current to be flown into the EL cell.

[0032] Said non-light-emitting period includes discharging the capacitor through a second switching transistor by an erasing scan signal from an erasing scan line; and turning off the driving transistor while turning on a backward bias transistor by a discharge of the capacitor, thereby applying said backward bias to the EL cell.

[0033] Herein, said light-emitting period includes turning off the driving transistor while turning on the backward bias transistor when said data signal is a non-light-emitting data, thereby applying said backward bias to the EL cell.

[0034] The backward bias transistor applies any one of said backward bias voltage and said erasing signal to the EL cell in the non-light-emitting period.

[0035] Herein, when the backward bias transistor supplies said erasing signal in the non-light-emitting period, said backward bias is applied to the EL cell only in a period when a turn-on voltage for turning on the second driving transistor by said erasing signal is supplied.

BRIEF DESCRIPTION OF THE DRAWINGS

[0036] These and other objects of the invention will be apparent from the following detailed description of the embodiments of the present invention with reference to the accompanying drawings, in which:

[0037] **FIG. 1** is a driving timing diagram of one frame according to a digital driving method of a general EL display panel;

[0038] **FIG. 2** is a detailed circuit diagram of one pixel configuring the related art EL display panel;

[0039] **FIG. 3** is a digital driving timing diagram of the EL display panel shown in **FIG. 2**;

[0040] **FIG. 4** is a detailed circuit diagram of one pixel of an EL display panel according to an embodiment of the present invention;

[0041] **FIG. 5** is a digital driving timing diagram of the EL display panel shown in **FIG. 4**;

[0042] **FIG. 6** is a detailed circuit diagram of one pixel of an EL display panel according to another embodiment of the present invention;

[0043] **FIG. 7** is a digital driving timing diagram of the EL display panel shown in **FIG. 6**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0044] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0045] Hereinafter, the preferred embodiments of the present invention will be described in detail with reference to **FIGS. 4** to **7**.

[0046] **FIG. 4** is a detailed circuit diagram of one pixel of an active matrix EL display panel for a digital driving according to an embodiment of the present invention, and **FIG. 5** is a driving timing diagram of the 1st sub-frame SF1 of a plurality of sub-frames SF1 to SF6.

[0047] Referring to **FIG. 4**, the pixel is comprised of an EL cell OLED, and a cell driver including three PMOS transistors P1, P2 and P3, a single of NMOS transistor N1 and a storage capacitor Cs for driving the EL cell OLED.

[0048] The cell driver includes a storage capacitor Cs connected to a power line PL, a first switching PMOS transistor P1 connected between a data line DL and the storage capacitor Cs to be controlled by a light-emitting scan

line SLp, a second switching PMOS transistor P2 connected between the power line PL and the storage capacitor Cs to be controlled by a non-light-emitting scan line SLe, a third driving PMOS transistor P3 connected between a voltage supply line VDD and the EL cell OLED to be controlled by the storage capacitor Cs, and a first NMOS transistor N1 connected between the storage capacitor and a backward bias voltage (V1) input line to be controlled by the storage capacitor Cs.

[0049] A writing scan line SLp provides a program signal PS for turning on the first PMOS transistor P1 in a light-emitting period LT of each sub-frame SF. The first PMOS transistor P1 is turned on by the program signal PS to charge the storage capacitor Cs, thereby turning on or off the third PMOS transistor P3 in accordance with the charged voltage during the light-emitting period LT; whereas the first NMOS transistor N1 is operated to the contrary. Thus, when the third PMOS transistor P3 is turned on in the light-emitting period LT, a high-level voltage VDD is supplied to the EL cell OLED such that a forward current is flown into the EL cell OLED, thereby light-emitting the EL cell OLED. On the other hand, when the first NMOS transistor N1 is turned on in the light-emitting period LT, a backward bias voltage V1 is supplied to the EL cell OLED to apply a backward bias to the EL cell OLED, thereby providing an aging of the EL cell OLED.

[0050] An erasing scan line SLe provides an erasing signal ES for turning on the second PMOS transistor P2 in a non-light-emitting period UT of each sub-frame SF, and the backward bias voltage (V1) input line supplies a direct current backward bias voltage V1 remaining at a low-level voltage as shown in **FIG. 5**. The second PMOS transistor P2 is turned on by the erasing signal SE to discharge the storage capacitor Cs, thereby turning on the third PMOS transistor P3 during the non-light-emitting period UT. On the other hand, the first NMOS transistor N1 is turned on to apply a backward bias to the EL cell OLED, thereby providing an aging of the EL cell OLED.

[0051] Referring to **FIG. 5**, the first PMOS transistor P1 is turned on by a low voltage of the program signal PS in the non-light-emitting period LT1 of the 1st sub-frame SF1. Further, a low voltage ("0") or a high voltage ("1") of the data signal is supplied via the turned-on first PMOS transistor P1, so that the data signal is charged in the storage capacitor Cs. When the low voltage of the data signal is charged in the storage capacitor Cs, the third PMOS transistor P3 is turned on during the light-emitting period LT such that a forward current is flown into the EL cell OLED, thereby light-emitting the EL cell OLED. On the other hand, when the high voltage of the data signal is charged in the storage capacitor Cs, the third PMOS transistor P3 is turned off while the first NMOS transistor N1 being turned on during the light-emitting period LT such that a backward bias is applied to the EL cell OLED, thereby providing an aging of the EL cell OLED.

[0052] Then, the second PMOS transistor P2 is turned on by a low voltage of the erasing signal SE in the non-light-emitting period UT1 to supply a high-level voltage VDD from the power line PL, thereby discharging the storage capacitor Cs. Thus, the third PMOS transistor P3 is turned off while the first NMOS transistor N1 being turned on during the non-light-emitting period UT1 such that a back-

ward bias is applied to the EL cell OLED, thereby providing an aging of the EL cell OLED.

[0053] As described above, the EL display panel according to the embodiment of the present invention applies a forward current when the EL cell OLED is light-emitted while applying a backward bias when the EL cell OLED is not light-emitted, so that it can prevent a life shortening of the EL cell OLED.

[0054] FIG. 6 is a detailed circuit diagram of one pixel in an EL display panel according to another embodiment of the present invention, and FIG. 7 is a driving timing diagram.

[0055] The pixel shown in FIG. 6 includes the same elements as the pixel shown in FIG. 4 except that the first NMOS transistor N1 for applying a backward bias employs an erasing signal ES as a backward bias voltage. Thus, a detailed explanation as to the same elements will be omitted.

[0056] The first NMOS transistor N1 shown in FIG. 6 is connected between the third PMOS transistor P3 and the erasing scan line SLe to be controlled by the storage capacitor Cs. If the second PMOS transistor P2 is turned on by a low voltage of the erasing signal ES in the non-light-emitting period UT1 as shown in FIG. 7, the first NMOS transistor N1 is turned on in opposition to the third PMOS transistor P3 due to a discharge of the storage capacitor Cs. The turned-on first NMOS transistor N1 supplies a low voltage of the erasing signal ES from the erasing scan line SLe to the EL cell OLED such that a backward current is flown into the EL cell OLED, thereby providing an aging of the EL cell OLED. Herein, the first NMOS transistor N1 allows a backward bias to be applied to the EL cell OLED only in a period when the low voltage of the erasing signal ES is supplied to the erasing scan line SLe.

[0057] For instance, when the erasing signal ES remains at a low voltage during the non-light-emitting period UT1 as shown in FIG. 7, the first NMOS transistor N1 allows a backward bias to be applied to the EL cell OLED during the non-light-emitting period UT1. On the other hand, when the erasing signal ES remains at a low voltage only in a portion of the non-light-emitting period UT1 as shown in FIG. 5, the first NMOS transistor N1 allows a backward bias to be applied to the EL cell OLED only in the low voltage period.

[0058] As described above, according to the present invention, a forward current is applied when the EL cell is light-emitted while a backward bias being applied when the EL cell is not light-emitted in the digital driving method, so that it becomes possible to prevent a life shortening of the EL cell caused by a direct current.

[0059] Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments, but rather that various changes or modifications thereof are possible without departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.

What is claimed is:

1. An electro-luminescence display panel implementing a gray level by a combination of light-emitting periods of sub-frames corresponding to each bit of video data, wherein each of pixels comprises:

an electro-luminescence (EL) cell; and

a cell driver for allowing a forward current to be flown into the EL cell in accordance with a supplied data signal in a light-emitting period of the sub-frame while allowing a backward bias to be applied to the EL cell in a non-light-emitting period of the sub-frame.

2. The electro-luminescence display panel according to claim 1, wherein the cell driver comprises:

a storage capacitor having one electrode connected to a power line;

a first switching transistor connected between a data line for supplying said data signal and other electrode of the storage capacitor to be controlled by a writing scan line for supplying a writing signal;

a second switching transistor connected to the power line and other electrode of the storage capacitor to be controlled by an erasing scan line for supplying an erasing signal;

a driving transistor connected between the power line and the EL cell to be controlled by the storage capacitor; and

a backward bias transistor connected between the driving transistor and a backward bias voltage input line to be controlled by the storage capacitor in opposition to the driving transistor.

3. The electro-luminescence display panel according to claim 2, wherein the first switching transistor is turned on by said writing signal in the light-emitting period to charge said data signal into the capacitor, and the second switching transistor is turned on by said erasing signal in the non-light-emitting period to discharge said data signal charged in the capacitor.

4. The electro-luminescence display panel according to claim 3, wherein the driving transistor turned on or off in accordance with said voltage charged in the capacitor in the light-emitting period while being turned off by said discharge of the capacitor in the non-light-emitting period, and allows said forward current to be flown into the EL cell when it is turned on in the light-emitting period.

5. The electro-luminescence display panel according to claim 3, wherein the backward bias transistor is turned on in opposition to the driving transistor in the non-light-emitting period, thereby applying said backward bias to the EL cell.

6. The electro-luminescence display panel according to claim 5, wherein the backward bias transistor is turned on when the driving transistor is turned off by said data signal charged in the capacitor in the light-emitting period, thereby applying said backward bias to the EL cell.

7. The electro-luminescence display panel according to claim 3, wherein the backward bias input line is identical to the erasing scan line.

8. The electro-luminescence display panel according to claim 7, wherein the erasing scan line applies a turn-on voltage of the second switching transistor as said erasing signal in the non-light-emitting period, and said backward bias is applied, via the backward bias transistor, to the EL cell during a period when said turn-on voltage of said erasing signal is applied.

9. The electro-luminescence display panel according to claim 2, wherein the first and second switching transistors

and the driving transistor are PMOS transistors, and the backward bias transistor is a NMOS transistor.

10. A method of driving an electro-luminescence display panel implementing a gray level by a combination of light-emitting periods of sub-frames corresponding to each bit of video data, said method comprising the steps of:

allowing a forward current to be flown into an electro-luminescence (EL) cell in accordance with a data signal in a light-emitting period of the sub-frame; and

allowing a backward bias to be applied to the EL cell in a non-light-emitting period of the sub-frame.

11. The method according to claim 10, wherein said light-emitting period includes:

allowing said backward bias to applied to the EL cell when a non-light-emitting data signal for non-light-emitting the EL cell by said data signal is supplied.

12. The method according to claim 11, wherein said light-emitting period includes:

allowing said data signal to be charged, via the first switching transistor, to a capacitor by a writing scan signal from a writing scan line; and

turning on a driving transistor in accordance with a voltage charged in the capacitor, thereby allowing said forward current to be flown into the EL cell.

13. The method according to claim 12, wherein said non-light-emitting period includes:

discharging the capacitor through a second switching transistor by an erasing scan signal from an erasing scan line; and

turning off the driving transistor while turning on a backward bias transistor by a discharge of the capacitor, thereby applying said backward bias to the EL cell.

14. The method according to claim 13, wherein said light-emitting period includes:

turning off the driving transistor while turning on the backward bias transistor when said data signal is a non-light-emitting data, thereby applying said backward bias to the EL cell.

15. The method according to claim 12, wherein the backward bias transistor applies any one of said backward bias voltage and said erasing signal to the EL cell in the non-light-emitting period.

16. The method according to claim 15, wherein, when the backward bias transistor supplies said erasing signal in the non-light-emitting period, said backward bias is applied to the EL cell only in a period when a turn-on voltage for turning on the second driving transistor by said erasing signal is supplied.

* * * * *

专利名称(译)	电致发光显示面板及其驱动方法		
公开(公告)号	US20050219169A1	公开(公告)日	2005-10-06
申请号	US11/094186	申请日	2005-03-31
[标]申请(专利权)人(译)	钟勋J JEON常^ h		
申请(专利权)人(译)	钟勋J JEON常^ h		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	CHUNG HOON JU JEON CHANG HOON		
发明人	CHUNG, HOON JU JEON, CHANG HOON		
IPC分类号	G09G3/30 G09G3/20 G09G3/32		
CPC分类号	G09G3/2022 G09G3/3258 G09G2300/0842 G09G2320/043 G09G2310/0251 G09G2310/0256 G09G2300/0861		
优先权	1020040022122 2004-03-31 KR		
其他公开文献	US8035580		
外部链接	Espacenet USPTO		

摘要(译)

公开了一种电致发光显示板及其驱动方法，用于防止由直流电引起的EL寿命缩短。在通过对应于每个视频数据位的子帧的发光周期的组合实现灰度级的电致发光显示面板中，每个像素包括电致发光（EL）单元和用于允许的单元驱动器在子帧的发光周期中根据所提供的数据信号流入EL单元的正向电流，同时允许在非发光周期中向EL单元施加反向偏置。子帧。

